

11/28/03

2 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
20263 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
7 6,321,285.pn. or 6,247,084.pn. or 6,088,753.pn. or 6,239,810.pn.
6 6,026,226.pn. or 6,510,541.pn. or 6,427,224.pn.
13 (6,321,285.pn. or 6,247,084.pn. or 6,088,753.pn. or 6,239,810.pn.) or (6,026,226.pn. or 6,51 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
6 ((6,321,285.pn. or 6,247,084.pn. or 6,088,753.pn. or 6,239,810.pn.) or (6,026,226.pn. or 6,5 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
3 ((6,321,285.pn. or 6,247,084.pn. or 6,088,753.pn. or 6,239,810.pn.) or (6,026,226.pn. or 6,5 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
2 (((6,321,285.pn. or 6,247,084.pn. or 6,088,753.pn. or 6,239,810.pn.) or (6,026,226.pn. or 6,5 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
20263 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
1 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
6 6,239,810.pn. or 5,594,874.pn. or 5,422,833.pn.
1 (6,239,810.pn. or 5,594,874.pn. or 5,422,833.pn.) and (bus with parameter with (change\$1 or USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
0 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
48 (((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3)) or (((digital or int USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
2 6,321,285.pn.
2 6,247,084.pn.
2 5,867,400.pn.
2 5,956,478.pn.
2 6,253,302.pn.
2 6,212,667.pn.

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Paul Bryan

EAST SEARCH

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Results of search set L10:(((digital or integrated) adj circuit) with (simulate\$3 or verification or verify\$3 or design)) and ((HDL or syntax) with (reduce\$1 or condense\$1 or simplify\$3))

Document Kind	Codes	Title	Issue Date	Current OR	Abstract
US 20030192023 A1		Apparatus and method for handling of multi-level circuit design data	20031009	716/11	
US 20030188272 A1		Synchronous assert module for hardware description language library	20031002	716/4	
US 20030144828 A1		Hub array system and method	20030731	703/21	
US 20030135832 A1		Method for creating a design verification test bench	20030717	716/5	
US 20030125925 A1		Batch editor for netlists described in a hardware description language	20030703	703/22	
US 20030070013 A1		Method and apparatus for reducing power consumption in a digital processor	20030410	710/59	
US 20030061580 A1		Simulation method and compiler for hardware/software programming	20030327	716/4	
US 20030033595 A1		Automated HDL modifying apparatus and computer-readable recording medium in which pro	20030213	717/143	
US 20020152060 A1		Inter-chip communication system	20021017	703/17	
US 20020138244 A1		Simulator independent object code HDL simulation using PLI	20020926	703/14	
US 20020078424 A1		Method for creating a design verification test bench	20020620	716/5	
US 20020059553 A1		Creating optimized physical implementations from high-level descriptions of electronic design	20020516	716/4	
US 20020049576 A1		Digital and analog mixed signal simulation using PLI API	20020425	703/14	
US 20020032894 A1		Design method for logic circuit, design support system for logic circuit and readable media	20020314	716/2	
US 6651239 B1		Direct transformation of engineering change orders to synthesized IC chip designs	20031118	716/18	
US 6651225 B1		Dynamic evaluation logic system and method	20031118	716/4	
US 6651224 B1		METHOD OF OPTIMIZING SIGNAL LINES WITHIN CIRCUIT, OPTIMIZING APPARATUS, F	20031118	716/2	
US 6622292 B2		Design method for logic circuit, design support system for logic circuit and readable media	20030916	716/9	
US 6606734 B2		Simulation method and compiler for hardware/software programming	20030812	716/4	
US 6587590 B1		Method and system for computing 8.times.8 DCT/IDCT and a VLSI implementation	20030701	382/250	
US 6499132 B1		System and method for analyzing temporal expressions	20021224	716/5	

US 6490711 B2	Method for creating a design verification test bench	20021203 716/5
US 6434733 B1	System and method for high-level test planning for layout	20020813 716/11
US 6421818 B1	Efficient top-down characterization method	20020716 716/18
US 6421251 B1	Array board interconnect system and method	20020716 361/788
US 6389379 B1	Converfication system and method	20020514 703/14
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423 716/18
US 6360356 B1	Creating optimized physical implementations from high-level descriptions of electronic design	20020319 716/18
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120 716/6
US 6295636 B1	RTL analysis for improved logic synthesis	20010925 716/18
US 6292931 B1	RTL analysis tool	20010918 716/18
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911 716/5
US 6289491 B1	Netlist analysis tool by degree of conformity	20010717 716/18
US 6263483 B1	Method of accessing the generic netlist created by synopsys design compiler	20010320 716/5
US 6205572 B1	Buffering tree analysis in mapped design	20010109 716/18
US 6173435 B1	Internal clock handling in synthesis script	2001107 716/18
US 6145117 A	Creating optimized physical implementations from high-level descriptions of electronic design	20001017 703/27
US 6134516 A	Simulation server system and method	20001017 717/131
US 6132109 A	Architecture and methods for a hardware description language source level debugging systier	20000919 710/52
US 6122680 A	Multiple channel data communication buffer with separate single port transmit and receive me	20000711 714/724
US 6088821 A	Logic circuit verification device for semiconductor integrated circuit	20000502 712/32
US 6058467 A	Standard cell, 4-cycle, 8-bit microcontroller	20000215 703/13
US 6026230 A	Memory simulation system and method	19991228 703/13
US 6009256 A	Simulation/emulation system and method	19991116 716/1
US 5987239 A	Computer system and method for building a hardware description language representation of	19990810 717/131
US 5937190 A	Architecture and methods for a hardware description language source level analysis and deb	19990727 716/8
US 5930147 A	Design support system in which delay is estimated from HDL description	19990202 716/1
US 5867400 A	Application specific processor and design method for same	19981006 716/10
US 5819072 A	Method of using a four-state simulator for testing integrated circuit designs having variable tir	19961105 716/18
US 5572712 A	Method and apparatus for making integrated circuits with built-in self-test	19960716 716/19
US 5537580 A	Integrated circuit fabrication using state machine extraction from behavioral hardware descrip	19950620 716/6
US 5426591 A	Apparatus and method for improving the timing performance of a circuit	19940329 716/18
US 5299137 A	Behavioral synthesis of circuits including high impedance buffers	20030731
US 20030144826 A	Integrated circuit design verifying method e.g. for application specific integrated circuit, involv	20030731
JP 2003216683 A	Functional verification apparatus for digital circuit e.g. CPU, generates verification information	21
US 20020138244 A	Hardware description language coded semiconductor integrated circuit simulation system cor	20020926
JP 2000163457 A	Circuit model verification apparatus used for designing of ASIC, LSIC, has verification block v	20000616
JP 09259154 A	Logic design method for semiconductor integrated circuit manufacture - by timing and analysi	11